

CLAIMS:

1. A semiconductor processing method comprising:

forming first and second layers over a substrate, the second layer having a higher oxidation rate than the first layer when exposed to an oxidizing atmosphere, the substrate having a periphery, the first layer having an exposed first outer edge spaced inside the substrate periphery, the second layer having an exposed first outer edge spaced inside the substrate periphery;

etching into the second layer first edge at a faster rate than any etching into the first layer first edge and forming an exposed second outer edge of the second layer; and

after the etching, exposing the substrate to the oxidizing atmosphere with the second layer second outer edge exposed and forming an oxidized first layer edge.

2. The method of claim 1 comprising forming the second layer over the first layer. - -

3. The method of claim 1 comprising forming the first layer over the second layer.

4. The method of claim 1 comprising forming the first and second layers to be electrically conductive.

1           5.    The method of claim 1 wherein the etching comprises wet  
2 etching.

3  
4           6.    The method of claim 1 wherein the etching comprises wet  
5 etching with a basic solution.

6  
7           7.    The method of claim 1 wherein the etching comprises wet  
8 etching with a solution comprising ammonium hydroxide and hydrogen  
9 peroxide.

10  
11           8.    The method of claim 1 further comprising forming a third  
12 layer over the first and second layers, the third layer having an exposed  
13 first outer edge spaced inside the substrate periphery, the third layer  
14 having a lower oxidation rate than the oxidation rate of the second  
15 layer when exposed to the oxidizing atmosphere, the etching into the  
16 second layer first edge forming the second layer second edge to be  
17 recessed inwardly relative to outer edges of both the first and third  
18 layers.

1           9.    A semiconductor processing method comprising:  
2           forming a stack of at least two conductive layers for an electronic  
3           component over a substrate, the two conductive layers having different  
4           oxidation rates when exposed to an oxidizing atmosphere, the layer with  
5           the higher oxidation rate having an outer lateral edge which is recessed  
6           inwardly of a corresponding outer lateral edge of the layer with the  
7           lower oxidation rate; and

8           exposing the stack of conductive layers to the oxidizing atmosphere  
9           effective to grow an oxide layer over the outer lateral edges of the  
10          first and second layers.

11  
12          10.   The method of claim 9 comprising forming the higher  
13          oxidation rate layer over the lower oxidation rate layer.

14  
15          11.   The method of claim 9 comprising forming the lower  
16          oxidation rate layer over the higher oxidation rate layer.

17  
18          12.   The method of claim 9 comprising forming another layer  
19          over the at least two conductive layers, the another layer having a  
20          lower oxidation rate than the layer having said higher oxidation rate  
21          when exposed to the oxidizing atmosphere, the outer lateral edge of the  
22          layer with said higher oxidation rate being recessed inwardly of a  
23          corresponding outer lateral edge of the another layer.

24

1           13. The method of claim 12 wherein the another layer is  
2 electrically insulative.

3  
4           14. The method of claim 9 wherein one of the at least two  
5 conductive layers comprises conductively doped polysilicon and another  
6 of the at least two conductive layers comprises a refractory metal  
7 silicide.

8  
9           15. A method of forming an electronic component comprising:  
10 forming first and second conductive materials over a substrate, the  
11 second material having a higher oxidation rate than an oxidation rate  
12 of the first material when exposed to an oxidizing atmosphere;

13 first etching the first and second conductive materials to form a  
14 conductive component, the conductive component having opposing  
15 substantially continuous straight linear outer lateral edges of the first  
16 and second conductive materials;

17 second etching into the second material outer lateral edges to  
18 recess them inside of the first material outer lateral edges; and

19 after the second etching, exposing the substrate to the oxidizing  
20 atmosphere effective to grow an oxide layer over the outer lateral edges  
21 of the first and second conductive materials.

1 16. The method of claim 15 one of the first and second  
2 conductive materials comprises conductively doped polysilicon and the  
3 other comprises a refractory metal silicide.

4  
5 17. The method of claim 15 wherein the second etching  
6 comprises wet etching.

7  
8 18. The method of claim 15 wherein the first etching comprises  
9 dry etching and the second etching comprises wet etching.

10  
11 19. The method of claim 15 wherein the second etching  
12 comprises wet etching with a basic solution.

13  
14 20. The method of claim 15 wherein the second etching  
15 comprises wet etching with a solution comprising ammonium hydroxide  
16 and hydrogen peroxide.

17  
18 21. The method of claim 15 comprising forming the second  
19 conductive material to be received over the first conductive material.

20  
21 22. The method of claim 15 wherein the first etching is  
22 conducted to space the opposing linear outer lateral edges less than 1  
23 micron apart from one another.

1           23. The method of claim 15 wherein the first etching is  
2 conducted to space the opposing linear outer lateral edges less than 1  
3 micron apart from one another, and further comprising ion implanting  
4 into the substrate proximate outer lateral edges of the first and the  
5 second conductive materials after the exposing.

6  
7           24. The method of claim 15 wherein the first etching is  
8 conducted to space the opposing linear outer lateral edges less than 1  
9 micron apart from one another, the second etching and the exposing  
10 being effective to form the oxide layer to have opposing substantially  
11 continuous straight linear outer lateral edges over the first and second  
12 conductive materials.

13  
14           25. The method of claim 24 wherein the opposing linear outer  
15 lateral edges of the oxide layer are formed to be less than 1 micron  
16 apart.

1           26. The method of claim 15 comprising forming a third  
2 insulative material over the first and second conductive materials, the  
3 first etching also etching the third insulative material to form the  
4 conductive component to have an insulative cap, the third insulative  
5 material having a lower oxidation rate than the second conductive  
6 material when exposed to the oxidizing atmosphere, the second etching  
7 recessing the second material outer lateral edges to within outer lateral  
8 edges of the third insulative material.

9  
10           27. The method of claim 26 wherein the first etching is  
11 conducted to form the insulative cap to have opposing outer lateral  
12 edges which are substantially straight continuously linear with the outer  
13 lateral edges of the first and second conductive materials, and the first  
14 etching is conducted to space said opposing linear outer lateral edges  
15 less than 1 micron apart from one another.

1           28. The method of claim 26 wherein the first etching is  
2 conducted to form the insulative cap to have opposing outer lateral  
3 edges which are substantially straight continuously linear with the outer  
4 lateral edges of the first and second conductive materials, and the first  
5 etching is conducted to space the opposing linear outer lateral edges  
6 less than 1 micron apart from one another, and further comprising ion  
7 implanting into the substrate proximate outer lateral edges of the first  
8 and the second conductive materials after the exposing.

9  
10           29. The method of claim 26 wherein the first etching is  
11 conducted to form the insulative cap to have opposing outer lateral  
12 edges which are substantially straight continuously linear with the outer  
13 lateral edges of the first and second conductive materials, and the first  
14 etching is conducted to space the opposing linear outer lateral edges  
15 less than 1 micron apart from one another, the second etching and the  
16 exposing being effective to form the oxide layer to have opposing  
17 substantially continuous-straight linear outer lateral edges over the first  
18 and second conductive materials.

19  
20           30. The method of claim 29 wherein the opposing linear outer  
21 lateral edges of the oxide layer are formed to be less than 1 micron  
22 apart.



1           31. A semiconductor processing method of forming a transistor  
2 comprising:

3           forming a gate dielectric layer, a doped silicon layer, a silicide  
4 layer and an insulating layer over a channel region of a substrate, the  
5 silicide layer having a higher oxidation rate than oxidation rates of the  
6 doped silicon layer and the insulating layer when exposed to an  
7 oxidizing atmosphere;

8           first etching the insulating layer, the silicide layer and the doped  
9 silicon layer to form a conductive gate stack having an insulating cap  
10 over the channel region, the gate stack having two opposing and  
11 respectively linearly aligned outer lateral edges of the insulating, silicide  
12 and doped silicon layers;

13           second etching the silicide layer substantially selectively relative to  
14 the insulating cap and the doped silicon layer to recess outer lateral  
15 edges of the silicide layer to within outer lateral edges of both the  
16 insulating and doped silicon layers of the gate stack;

17           after the second etching, exposing the substrate to the oxidizing  
18 atmosphere effective to grow an oxide layer over outer lateral edges of  
19 the silicide and doped silicon layers;

20           after the exposing, first implanting a dopant impurity into the  
21 substrate proximate the gate stack to form at least one of an LDD  
22 region or a halo region;

23           after the first implanting, forming insulative material over the  
24 oxide layer; and

1 after forming the insulative material, second implanting a dopant  
2 impurity into the substrate proximate the gate stack to form transistor  
3 source/drain regions.

4  
5 32. The method of claim 31 wherein the first etching is  
6 conducted to space the opposing substantially linear outer lateral edges  
7 less than 1 micron apart from one another.

8  
9 33. The method of claim 31 wherein the first etching is  
10 conducted to space the opposing linear outer lateral edges less than 1  
11 micron apart from one another, the second etching and the exposing  
12 being effective to form the oxide layer to have opposing substantially  
13 continuous straight linear outer lateral edges over the insulating, silicide  
14 and doped silicon layers.

15  
16 34. The method of claim 33 wherein the opposing linear outer  
17 lateral edges of the oxide layer are formed to be less than 1 micron  
18 apart.

19  
20 35. The method of claim 31 wherein the second etching  
21 comprises wet etching.  
22  
23  
24

1           36.   The method of claim 31 wherein the first etching comprises  
2 dry etching and the second etching comprises wet etching.

3  
4           37.   The method of claim 31 wherein the second etching  
5 comprises wet etching with a basic solution.

6  
7           38.   The method of claim 31 wherein the second etching  
8 comprises wet etching with a solution comprising ammonium hydroxide  
9 and hydrogen peroxide.  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24

1 39. A transistor comprising:

2 a semiconductive substrate;

3 a stack of a gate dielectric layer over the semiconductive  
4 substrate, a first conductive layer over the gate dielectric layer, a  
5 second conductive layer different in composition from the first and  
6 received over the first, and an insulative cap over the second conductive  
7 layer; the first conductive layer of the stack having opposing outer  
8 lateral edges which are spaced less than one micron apart defining a  
9 channel length within the semiconductive substrate of less than one  
10 micron, the second conductive layer of the gate stack having opposing  
11 outer lateral edges which are spaced apart less than the opposing outer  
12 lateral edges of the first conductive layer are spaced apart; and

13 an oxide layer formed over the outer lateral edges of the first  
14 conductive layer, the second conductive layer and the insulative cap, the  
15 oxide layer having opposing substantially continuous straight linear outer  
16 lateral edges over the insulating cap, the first conductive layer and the  
17 second conductive layer.

18  
19 40. The transistor of claim 39 wherein the opposing linear outer  
20 lateral edges of the oxide layer are formed to be less than 1 micron  
21 apart.  
22  
23  
24

1           41. The transistor of claim 39 wherein the oxide layer has a  
2 lateral thickness of less than 100 Angstroms over the first conductive  
3 layer.

4  
5           42. The transistor of claim 39 wherein the oxide layer has a  
6 lateral thickness of less than 100 Angstroms and greater than  
7 10 Angstroms over the first conductive layer.

8  
9           43. A transistor comprising:  
10 a semiconductive substrate;  
11 a gate stack formed over the semiconductive substrate and defining  
12 in at least one cross section a channel length within the semiconductive  
13 substrate of less than 1 micron, the gate stack comprising conductive  
14 material formed over a gate dielectric layer; and  
15 an insulative layer formed on outer lateral edges of the conductive  
16 material, the insulative layer having opposing substantially continuous  
17 straight linear outer lateral edges over all conductive material of the  
18 gate stack within the one cross section.

19  
20           44. The transistor of claim 43 wherein the opposing linear outer  
21 lateral edges of the insulative layer are formed to be less than 1  
22 micron apart.  
23  
24

1           45. The transistor of claim 43 wherein the insulative layer has  
2 a minimum lateral thickness of less than 100 Angstroms over said all  
3 conductive material.

4  
5           46. The transistor of claim 43 wherein the insulative layer has  
6 a minimum lateral thickness of less than 100 Angstroms and greater  
7 than 10 Angstroms over said all conductive material.

8  
9           47. The transistor of claim 43 wherein the conductive material  
10 comprises at least two conductive layers, the conductive layers within the  
11 one cross section of the gate stack having opposing outer lateral edges  
12 which are displaced from one another.